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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,772	09/12/2003	Makoto Shizukuishi	107317-00061	5771

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EXAMINER	
LIVEDALEN, BRIAN J	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,772	SHIZUKUISHI, MAKOTO	
	Examiner	Art Unit	
	Brian J. Livedalen	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 09/12/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5, 6, 15, 16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (US 6501109) in view of Suzuki (US 6816198).

Regarding claim 1, Chi discloses (fig 3b) a solid state image pickup device having a semiconductor substrate having a first layer of a first conductivity type (70); a second layer of a second conductivity type opposite to the first conductivity type (40), said second conductivity type layer being formed on the first conductivity type layer of said semiconductor substrate; a first region of the first conductivity type formed in said second conductivity type layer and constituting a photodiode with said second conductivity type layer (38); a first gate structure (44) including a charge storage region and a control gate, said first gate structure on a side opposite to said first region, and constituting a nonvolatile memory element with said first region and said first gate structure (column 3, lines 10-30). Chi is silent regarding a control circuit for applying a write voltage to the control gate. Suzuki discloses (fig 2) a control circuit (29) for applying a write voltage to the control gate, which can be a tunneling voltage (column 4, lines 16-20). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to include the control means of Suzuki to the image pickup device of Chi in order to control the read and write functions of the image pickup device.

In regard to claim 2, Chi in view of Suzuki discloses a control circuit, which can also apply a second voltage to the control gate being a hot carrier injection voltage (column 4, lines 20-27).

In regard to claim 5, Chi in view of Suzuki discloses the charge storage region having a floating gate (column 3, lines 20-21).

In regard to claim 6, Chi in view of Suzuki discloses the charge storage region having an interface between a silicon nitride film and a silicon oxide film (column 7, lines 19-37).

In regard to claim 15, Chi discloses (fig 3b) a solid state image pickup device having a semiconductor substrate having a first layer of a first conductivity type (70); a second layer of a second conductivity type opposite to the first conductivity type (40), said second conductivity type layer being formed on the first conductivity type layer of said semiconductor substrate constituting a photodiode. Chi discloses light being applied to the photodiode and a control gate (44) of a nonvolatile memory element having a charge storage region and a drain; and nonvolatile memory element is disposed adjacent to the photodiode (column 3, lines 10-30). Chi is silent regarding a control circuit to apply read and write voltages. Suzuki discloses (fig 2) a control circuit (29) for applying a write voltage to the control gate, which can be a tunneling voltage (column 4, lines 16-20) and a read voltage (column 4, lines 54-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include

the control means of Suzuki to the image pickup device of Chi in order to control the read and write functions of the image pickup device.

In regard to claim 16, Chi in view of Suzuki discloses a method using a control circuit, which can also apply a second voltage to the control gate being a hot carrier injection voltage (column 4, lines 20-27).

In regard to claim 20, Chi in view of Suzuki discloses a method using a control circuit, which can apply a reverse voltage to the substrate to drain charges on the photodiode to the substrate (column 4, lines 40-45).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (US 6501109) in view of Suzuki (US 6816198) as applied to claim 1 above, and further in view of Yamauchi et al (5075888).

In regard to claim 3, Chi in view of Suzuki discloses an image pickup device with a control circuit. Chi in view of Suzuki is silent regarding a third region of the first conductivity type formed adjacent to a side of a second insulated gate structure opposite the first region constituting an insulated gate type transistor or a control means to turn on the transistor. Yamauchi discloses (fig 9) a third region (1) and a gate (G1) that constitute an insulated gate type transistor with the first region. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the insulated gate type transistor of Yamauchi to the image pickup device of Chi in view of Suzuki in order to improve the speed of the voltage rewrite function.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (US 6501109) in view of Suzuki (US 6816198) as applied to claim 15 above, and further in view of Yamauchi et al (5075888).

In regard to claim 17, Chi in view of Suzuki discloses an image pickup device with a control circuit. Chi in view of Suzuki is silent regarding a third region of the first conductivity type formed adjacent to a side of a second insulated gate structure opposite the first region constituting an insulated gate type transistor or a control means to turn on the transistor. Yamauchi discloses (fig 9) a third region (1) and a gate (G1) that constitute an insulated gate type transistor with the first region and a controlling means, which turns on the transistor in order to apply a voltage to the nonvolatile memory element and charge said element (column 7, lines 66-68). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the insulated gate type transistor of Yamauchi to the image pickup device of Chi in view of Suzuki in order to improve the speed of the voltage rewrite function and supply current to the nonvolatile memory element.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (US 6501109) in view of Suzuki (US 6816198) as applied to claim 15 above, and further in view of Lee et al. (US 2004/0214379).

In regard to claim 18, Chi in view of Suzuki discloses a method for driving a image pickup device. Chi in view of Suzuki does not disclose applying a forward bias to the first region of the substrate to supply a current to the nonvolatile memory element.

Lee discloses applying a forward bias to the first region of the substrate to supply a current to the nonvolatile memory element (page 15, 2nd column). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the applying a forward bias to the first region of Lee to the method of Chi in view of Suzuki to allow tunneling to occur.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (US 6501109) in view of Suzuki (US 6816198) as applied to claim 15 above, and further in view of Chi et al (6060742).

In regard to claim 19, Chi in view of Suzuki discloses a method for driving a image pickup device. Chi in view of Suzuki does not disclose applying a forward bias to the first region of conductivity type projecting from an upper surface of the first conductivity type layer of the semiconductor substrate into the second conductivity type layer to supply a channel current to the non-volatile memory element. Chi et al does disclose applying a forward bias to the first region of conductivity type projecting from an upper surface of the first conductivity type layer of the semiconductor substrate into the second conductivity type layer to supply a channel current to the non-volatile memory element (column 5, lines 10-19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include applying a forward bias to the third region of Chi et al. to the image pickup device of Chi in view of Suzuki in order to increase electron injecting efficiency.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (US 6501109) in view of Suzuki (US 6816198) as applied to claim 1 above, and further in view of Chi et al (6060742).

In regard to claim 4, Chi in view of Suzuki discloses an image pickup device with a control circuit. Chi in view of Suzuki is silent regarding a third region of the first conductivity type projecting from an upper surface of the first conductivity type layer of the semiconductor substrate into the second conductivity layer. Chi et al. discloses (fig. 6) a region of the first conductivity type projecting from an upper surface of the first conductivity type layer of the semiconductor substrate into the second conductivity layer (603). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the third region of Chi et al. to the image pickup device of Chi in view of Suzuki in order to provide a channel between the drain and the source and a resulting higher electron injecting efficiency.

Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (US 6501109) in view of Yamauchi et al (5075888).

In regard to claim 7, Chi discloses (fig 3b) a solid state image pickup device having a semiconductor substrate having a first layer of a first conductivity type (70); a second layer of a second conductivity type opposite to the first conductivity type (40), said second conductivity type layer being formed on the first conductivity type layer of said semiconductor substrate; a first region of the first conductivity type formed in said second conductivity type layer and constituting a photodiode with said second conductivity type layer (38); a first gate structure (44) including a charge storage region

and a control gate, said first gate structure on a side opposite to said first region, and constituting a nonvolatile memory element with said first region and said first gate structure (column 3, lines 10-30). Chi is silent regarding a third region of the first conductivity type formed adjacent to a side of a second insulated gate structure opposite the first region constituting an insulated gate type transistor. Yamauchi discloses (fig 9) a third region (1) and a gate (G1) that constitute an insulated gate type transistor with the first region. It would have been obvious to on of ordinary skill in the art at the time the invention was made to include the insulated gate type transistor of Yamauchi to the image pickup device of Chi in order to improve the speed of the voltage rewrite function.

In regard to claim 8, Chi in view of Yamauchi discloses a controlling means, which turns on the transistor in order to apply a voltage to the nonvolatile memory element and charge said element (column 7, lines 66-68).

In regard to claim 9, Chi in view of Yamauchi discloses the charge storage region having a floating gate (column 3, lines 20-21).

In regard to claim 10, Chi in view of Yamauchi discloses the charge storage region having an interface between a silicon nitride film and a silicon oxide film (column 7, lines 19-37).

Claims 11, 13, and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (US 6501109) in view of Lee et al. (US 2004/0214379).

In regard to claim 11, Chi discloses (fig 3b) a solid state image pickup device having a semiconductor substrate having a first layer of a first conductivity type (70); a second layer of a second conductivity type opposite to the first conductivity type (40), said second conductivity type layer being formed on the first conductivity type layer of said semiconductor substrate; a first region of the first conductivity type formed in said second conductivity type layer and constituting a photodiode with said second conductivity type layer (38); a first gate structure (44) including a charge storage region and a control gate, said first gate structure on a side opposite to said first region, and constituting a nonvolatile memory element with said first region and said first gate structure (column 3, lines 10-30). Chi is silent regarding a control circuit to control the voltage. Lee discloses (fig 30) a control circuit for applying a voltage to a substrate (page 15, 2nd column). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the control means of Lee to the image pickup device of Chi in order to control the supply current of the nonvolatile memory element.

In regard to claim 13, Chi in view of Lee discloses the charge storage region having a floating gate (column 3, lines 20-21).

In regard to claim 14, Chi in view of Lee discloses the charge storage region having an interface between a silicon nitride film and a silicon oxide film (column 7, lines 19-37).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chi (US 6501109) in view of Lee et al. (US 2004/0214379) as applied to claim 11 above, and further in view of Chi et al (6060742).

In regard to claim 12, Chi in view of Lee discloses an image pickup device with a control circuit. Chi in view of Lee is silent regarding a third region of the first conductivity type projecting from an upper surface of the first conductivity type layer of the semiconductor substrate into the second conductivity layer. Chi et al. discloses (fig. 6) a region of the first conductivity type projecting from an upper surface of the first conductivity type layer of the semiconductor substrate into the second conductivity layer (603). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the third region of Chi et al. to the image pickup device of Chi in view of Lee in order to provide a channel between the drain and the source and a resulting higher electron injecting efficiency.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Livedalen whose telephone number is (571) 272-2715. The examiner can normally be reached on 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bjl

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